

# **MS8503DEP**

## **A Caller ID Integrated System with OTP ROM**

Features .....	1
Block Diagram .....	1
Application.....	1
Package .....	1
General Description .....	1
Pin Configuration.....	2
Pin Description.....	2
Absolute Maximum Ratings .....	5
AC & DC Electrical Characteristics .....	5
Bonding Diagram .....	7
Package Diagram .....	9

Notice: MSHINE's products are sold by description only, MSHINE reserves the rights to make changes in circuit design and/or specification at any time without notice. Accordingly, the reader is cautioned to make sure the latest version of data sheets are available before placing orders.

### **M-Shine Technologies Corporation**

#### **HEAD QUARTER**

2F, No.1008, Sec.4, Jhongsing Rd,  
Jhudong Township,Hsinchu, 310, Taiwan  
Tel: 886-3-5833899 Fax: 886-3-5830858

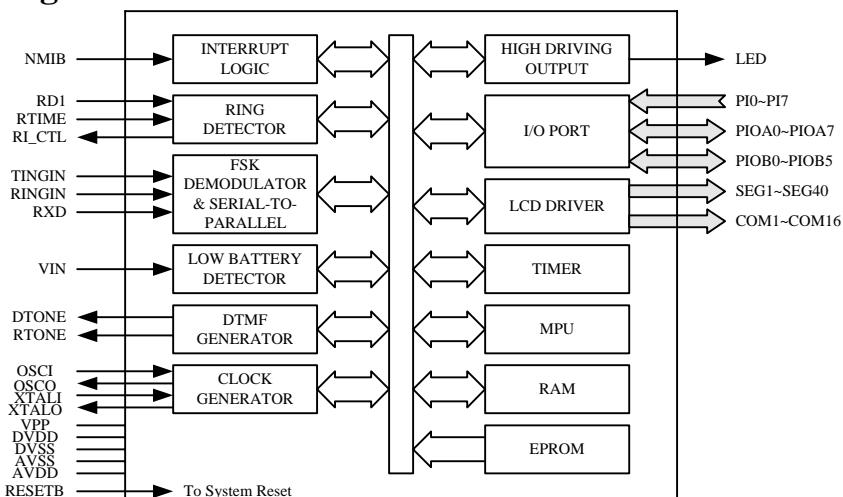
#### **SHENZHEN OFFICE**

Tel:86-755-88250870 Fax:86-755-88250872

## Features

- 8-bit micro-processor built in
- 32K bytes OTP (One Time Programming) ROM
- 2K bytes genera-purposed RAM
- Dual oscillator
  - 3.58MHz for system clock
  - 32.768KHz for system clock and real time clock
- Ring detector with line reversal detected
- FSK demodulator & carrier detector
- DTMF generator
- Ringer tone generator
- Low voltage detector
- Interrupts with three priorities and NMI
- Two general-purposed 8-bit timers
- Watchdog Timer
- Two serial-to-parallel ports
- I/O ports with internal pull-up resistors built in
  - Input port : 8 pins
  - I/O port A: 8 pins with/without open-drain option
  - I/O port B: 6 pins
- Other output pins
  - RI\_CTL pin, LED pin
- One LCD driver
  - two option bias: 1/5 or 1/4 by programming
  - three optional duty: 1/16, 1/8 or 1/4 by programming:
    - 40 segments × 16 commons (1/16 duty)
    - 40 segments × 8 commons (1/8 duty)
    - 40 segments × 4 commons (1/4 duty)
- Two power saving mode
  - Standby mode
  - Stop mode
- Operating voltage range: 2.8V~5.5V

## Block Diagram



## Application

- Calling number delivery (CND) and calling name delivery (CNAM) features
- Phone set adjunct boxes
- Feature phones
- Other communication systems

## Package

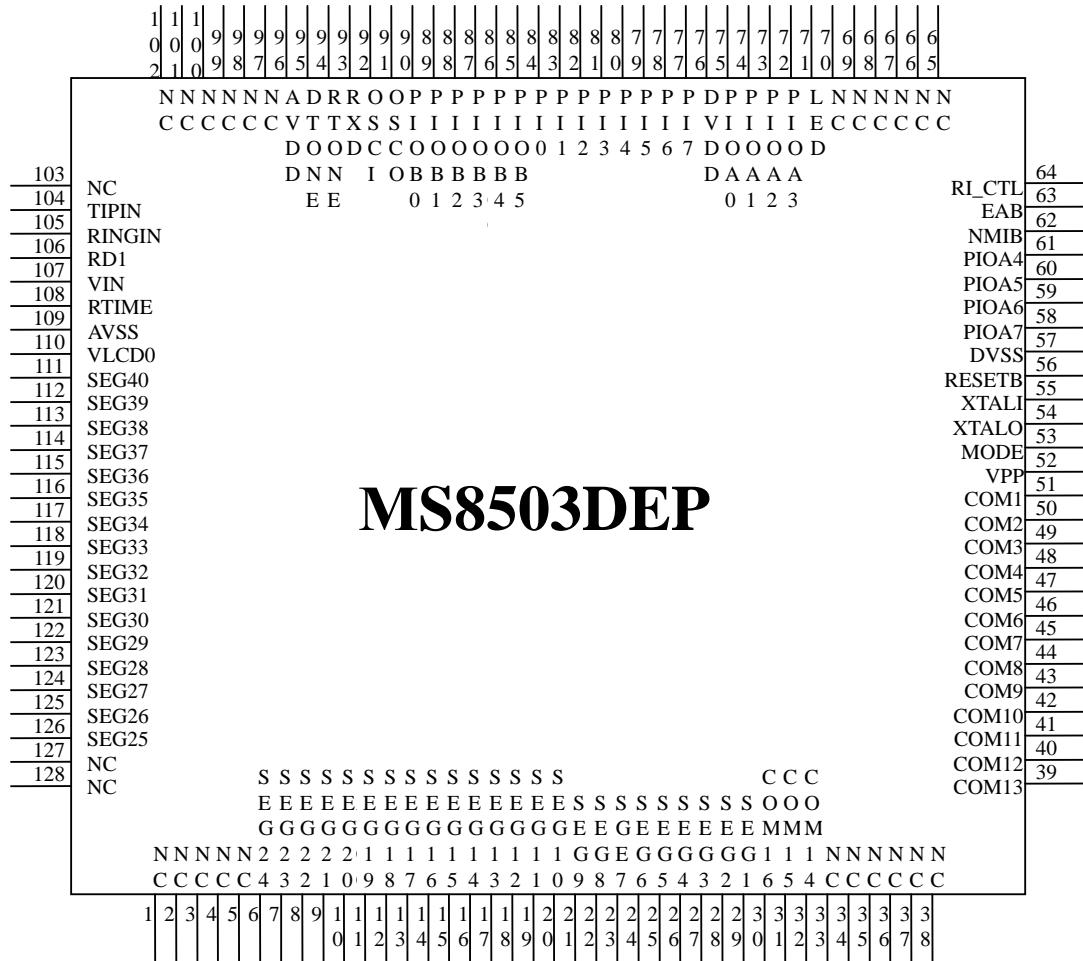
- 128-pin QFP packaged

## General Description

The MS8503DEP is the OTP (One Time Programming) version of the MS8503C series. It is a micro-controller with an 8-bit micro-processor (6502) embedded and it provides a complete solution for the service of caller identification. The features and functions offered by the MS8503DEP include FSK demodulation, DTMF generation, Ring detection, LCD driver, Power Management and Low battery indication. The FSK demodulator is designed for the Bell 202 and CCITT V.23 1200-baud asynchronous data and its performance is compliant to the Bellcore GR-30-CORE. With 32K Bytes ROM embedded, it can help the designers easily and flexibly to achieve

the desired features. For these applications, it provides a one-chip solution for the adjunct boxes, feature phones, and other communication systems.

## Pin Configuration



## Pin Description

### **Normal Pins (for IC operating in the normal mode)**

Pin No.	Notation	I/O	Description
6-29	SEG24 – SEG1	O	Segment output pins of LCD driver.
30-32	COM16 – COM14	O	Common output pins of LCD driver.
39-51	COM13 – COM1	O	Common output pins of LCD driver.
52	VPP	POWER	OTP Programming mode power input (10.65 volts / 5.6 volts). Note that when IC operating in normal mode, VPP must be connected to DVDD.
53	MODE	I	This pin specifies the IC operating mode: High: IC works in normal mode. Low: IC works in programming mode.
54	XTALO	O	32.768KHz oscillator output.
55	XTALI	I	32.768KHz oscillator input.
56	RESETB	I	Reset signal input (low active).
57	DVSS	POWER	Digital ground input.

58-61	PIOA7 – PIOA4	I/O	General-purposed I/O pins with internal pull-up resistors. Open-drain structure is optioned by masking.
62	NMIB	I	Non-maskable Interrupt input with schmitt trigger built in (low active).
63	EAB	I	This is a reserved pin with internal pull-up resistors. Don't connect this pin to any specified level.
64	RI_CTL	O	Ring control output or general-purposed output.
71	LED	O	General-purposed output with high driving capability (Max. 10 - 15 mA).
72-75	PIOA3 – PIOA0	I/O	General-purposed I/O pins with internal pull-up resistors. Open-drain structure is optioned by masking.
76	DVDD	POWER	Digital power supply input.
77-84	PI7 – PI0	I	General-purposed input pins with internal pull-up resistors. It can be programmed as interrupt input (negative-edge trigger).
85-90	PIOB5 – PIOB0	I/O	General-purposed I/O pins with internal pull-up resistors.
91	OSCO	O	3.58MHz oscillator output.
92	OSCI	I	3.58MHz oscillator input.
93	RXD	I	This pin is used to receive the output data of external FSK demodulator. One internal serial-to-parallel port is connected to this pin.
94	RTONE	O	Ringer tone signal output.
95	DTONE	O	DTMF signal output.
96	AVDD	POWER	Analog power supply input.
104	TIPIN	I	Signal input of ring side of twisted pair line (*see note 1).
105	RINGIN	I	Signal input of ring side of twisted pair line (*see note 1).
106	RD1	I	Ring detection signal input (*see note 2).
107	VIN	I	Low-voltage detector input.
108	RTIME	I	Ring time signal input.
109	AVSS	Power	Analog ground input.
110	VLCD0	I	Voltage supply input for LCD driver.
111-126	SEG40 – SEG25	O	Segment output pins of LCD driver.

Note 1: 'TIPIN' and 'RINGIN' must be DC isolated from the phone line.

Note 2: 'RD1' input is normally coupled to the one of the twisted pair wires through an attenuating network. It detects energy and enables the 3.58MHz oscillator and precision ring detection.

Note 3: It is suggested that the power AVDD and DVDD are blocked by coil for de-coupling the noise form analog circuit to digital circuit. (AVSS and DVSS, too)

**OTP ROM Programming Pins (for IC operating in the OTP programming mode)**

Pin No.	Programming Mode Notation	Notation	I/O	Description
29	SCLK	SEG1	I	Serial clock input (1MHz).
28	DI	SEG2	I	Serial data input (normal high).
27	PGMB	SEG3	I	The enabling of Programming Logic. Asserting PGMB to low will enable it.
26	OEB	SEG4	I	The enabling of Output Enable Logic. Asserting OEB to low will enable it.
25	IncAddrB	SEG5	I	Each low pulse of this signal will increase one programming address (normal high).
24	CompOKB/DO	SEG6	O	This is a multi-function output pin: CompOKB: Low: The result of Compare Logic is correct. High: The result of Compare Logic is incorrect. DO: Serial data output.
52	Vpp	Vpp	Power	Programming power input (10.65 volts / 5.6 volts).
53	MODE	MODE	I	This pin specifies the IC operating mode: High: IC works in normal mode. Low: IC works in programming mode.

Note: When IC operating in normal mode, only power 'VPP' and pin 'MODE' must be connected. Other pins ('SCLK', 'DI', 'PGMB', 'OEB', 'InAddrB', and 'CompOKB/DO') are used as the segment output pins of LCD Driver. In normal mode, pin 'MODE' must be connected to high state while power 'VPP' must be connected to power 'DVDD'.

## Absolute Maximum Ratings

DC Supply Voltage.....-0.5V to + 6.0V  
 Input Voltage.....-0.5V to  $V_{DD}$  + 0.5V  
 Output Voltage.....-0.5V to  $V_{DD}$  + 0.5V  
 Operating Temperature.....0°C to 70°C  
 Storage Temperature.....-40°C to 150°C

### Comments

Never allow a stress to exceed the values listed under "Absolute Maximum Ratings", otherwise the device would suffer from a permanent damage. Nor is a stress at the listed value be allowed to persist over a period, since an extended exposure to the absolute maximum rating condition may also affect the reliability of the device, if not causing a damage thereof.

## AC & DC Electrical Characteristics

### DC Electrical Characteristics

(Temperature=0°C to 70°C,  $V_{DD}$ =4.5V, GND=0V)

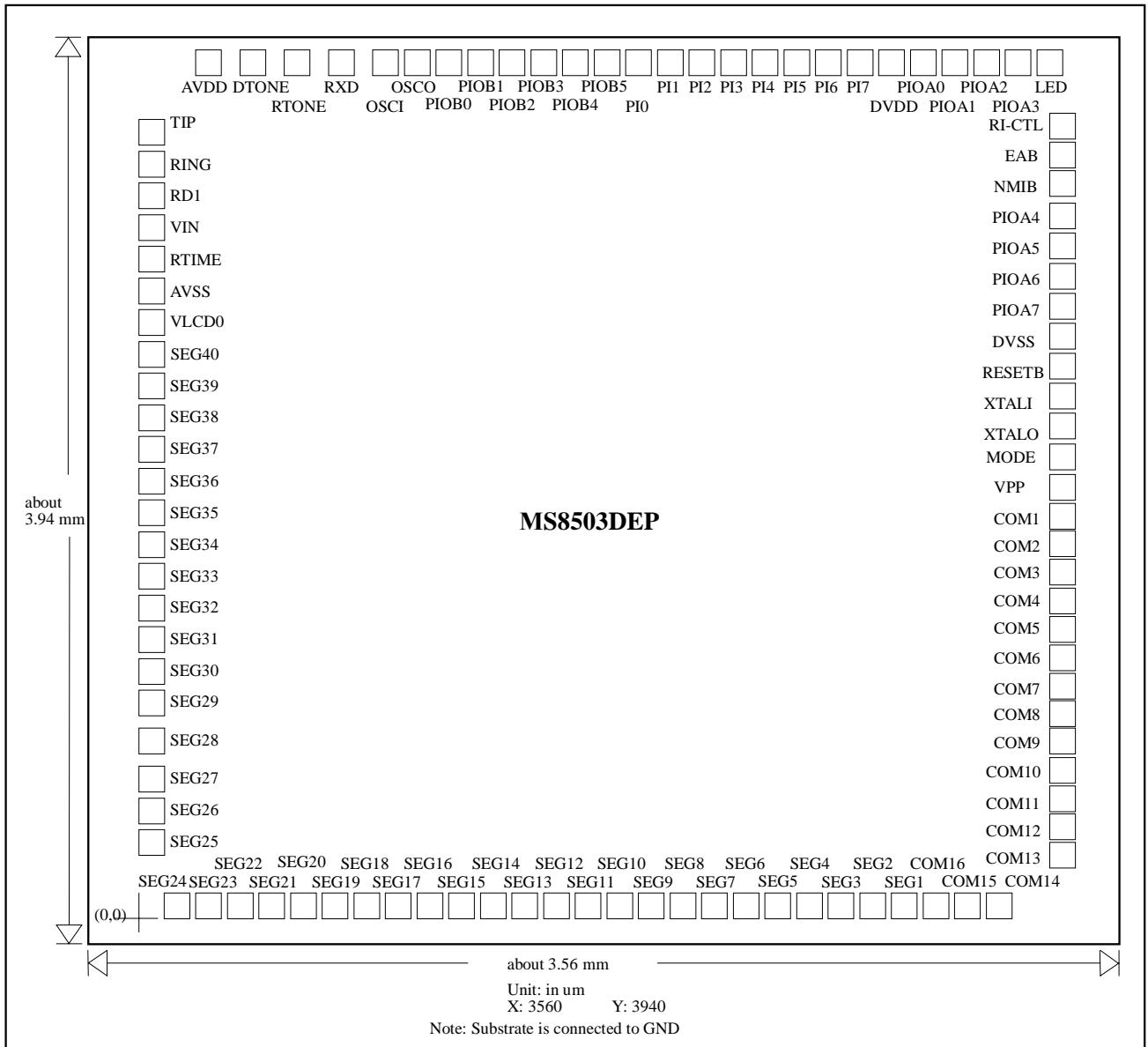
Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	MPU operating voltage	$V_{DD}$	2.2	5.0	5.5	V
	FSK operating voltage	$V_{DDF}$	2.8	5.0	5.5	V
	RAM operating voltage	$V_{RAM}$	2.2	5.0	5.5	V
Output voltage	$I_{OH}=1$ mA , PIOA and PIOC pins	$V_{OH1}$	4.3	-	-	V
	$I_{OL}=2$ mA, PIOA and PIOC pins	$V_{OL1}$	0.2	-	-	V
	$I_{OL}=2.2$ mA, PIOA open-drained	$V_{OL2}$	0.2	-	-	V
Input voltage	PIOA and PIOC pins	$V_{IH1}$	0.8 $V_{DD}$	-	$V_{DD}+0.3$	V
	PIOA and PIOC pins	$V_{IL1}$	-0.3	-	0.2 $V_{DD}$	V
	PI pins	$V_{IH2}$	0.8 $V_{DD}$	-	$V_{DD}+0.3$	V
	PI pins	$V_{IL2}$	-0.3	-	0.1 $V_{DD}$	V
Output current	$V_{OH}=4.0$ V, PIOA and PIOC pins	$I_{OH1}$	-2.4	-2.6	-2.7	mA
	$V_{OH}=3.6$ V		-4.0	-4.4	-4.6	
	$V_{OH}=0.9$ V, PIOA and PIOC pins	$I_{OL1}$	6.3	7.00	7.4	mA
	$V_{OH}=0.5$ V		3.9	4.4	4.6	
Pull-up resistor	$V_{OH}=0.9$ V, PIOA open-drained	$I_{OL2}$	7.2	8.0	8.5	mA
	$V_{OH}=0.5$ V		4.5	5.0	5.3	
DTMF output distortion	$R_{load}=10K\Omega \sim 40K\Omega$	DIS	-	-	0.7	%
Twist of DTMF power (high freq. power-low freq. power)	$R_{load}=10K\Omega \sim 40K\Omega$	TW	1	2	3	dB
DTMF loading resistor	-	$R_{load}$	5	10	40	KΩ

### AC Electrical Characteristics

(Temperature=0°C to 70°C, V<sub>DD</sub>=4.5V, GND=0V)

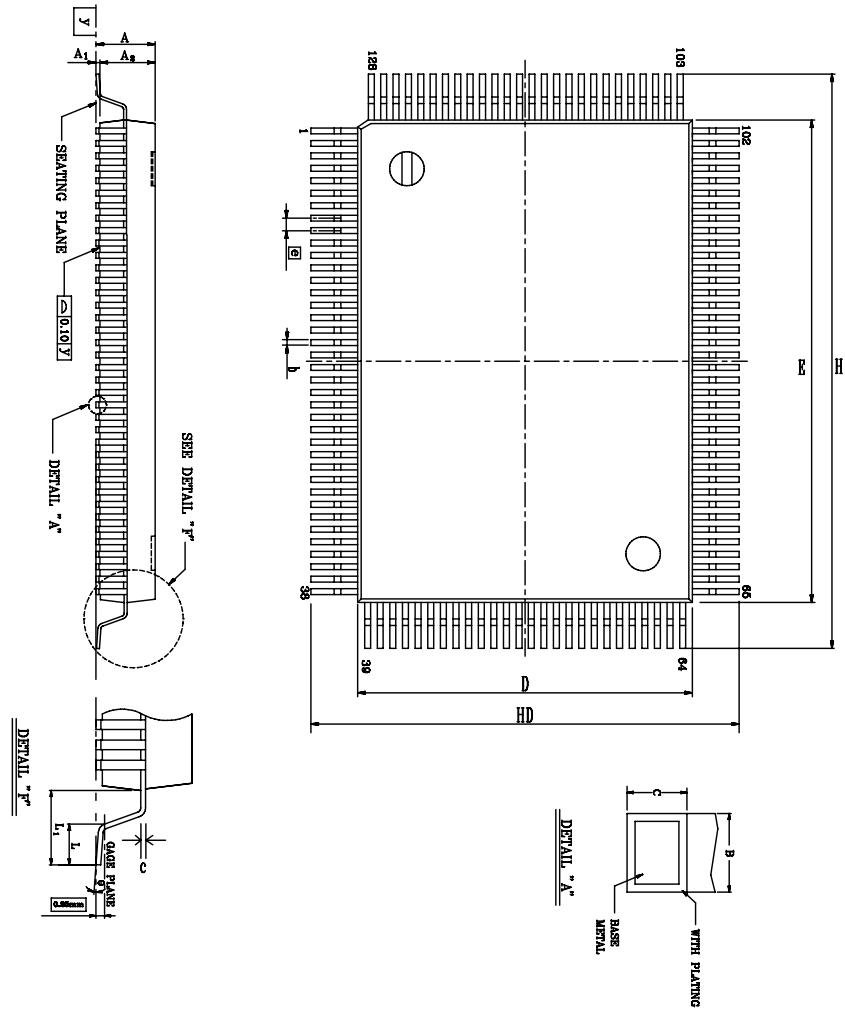
Parameters	Conditions	Min.	Typ.	Max.	Unit
Input sensitivity of Tip and Ring	S/N=25, Baud rate=1200 Bps Mark=1200Hz, Space=2200Hz	-	-45	-	dBm
SNR of input signal	Signal level = 0~-45dBm Baud rate=1200 Bps Mark=1200Hz, Space=2200Hz	-	11	-	dB
Baud Rate	Signal level = -45dBm, S/N>=22 Mark=1200Hz, Space=2200Hz	1150	1200	1250	Bps
Positive twist (twist = mark power-space power) Negative twist	Signal level=-45dBm, S/N>=22, Baud rate=1200Bps Signal level=-45dBm, S/N>=27, Baud rate=1200Bps	-	+10 -10	-	dB
Bell 202 FSK Mark frequency Space frequency	Signal level=-45dBm, S/N>=12 Baud rate=1200Bps	1200-1.0% 2200-1.0%	1200 2200	1200+1.0% 2200+1.0%	Hz
	Signal level=-45dBm, S/N>=14 Baud rate=1200Bps	1200-100 2200-100	1200 2200	1200+100 2200+100	Hz
CCITT V.23 FSK Mark frequency Space frequency	Signal level=-45dBm, S/N>=12 Baud rate=1200Bps	1300-1.0% 2100-1.0%	1300 2100	1300+1.0% 2100+1.0%	Hz
	Signal level=-45dBm, S/N>=14 Baud rate=1200Bps	1300-100 2100-100	1300 2100	1300+100 2100+100	Hz

## Bonding Diagram



<b>Pad No.</b>	<b>Name</b>	<b>X</b>	<b>Y</b>	<b>Pad No.</b>	<b>Name</b>	<b>X</b>	<b>Y</b>
1	TIP	86.04	3685.80	52	COM12	3467.43	290.60
2	RING	86.04	3560.22	53	COM11	3467.43	421.01
3	RD1	86.04	3440.16	54	COM10	3467.43	553.15
4	VIN	86.04	3320.10	55	COM9	3464.93	682.93
5	RTIME	86.04	3200.02	56	COM8	3464.93	809.94
6	AVSS	86.04	3079.97	57	COM7	3464.93	937.00
7	VLCDO	86.04	2907.55	58	COM6	3464.93	1064.21
8	SEG40	86.04	2742.65	59	COM5	3464.93	1191.47
9	SEG39	86.04	2575.34	60	COM4	3464.93	1318.63
10	SEG38	86.04	2408.03	61	COM3	3464.93	1445.79
11	SEG37	86.04	2242.87	62	COM2	3464.93	1572.90
12	SEG36	86.04	2078.32	63	COM1	3464.93	1700.06
13	SEG35	86.04	1913.67	64	VPP	3472.95	1965.23
14	SEG34	86.04	1747.21	65	MODE	3464.94	2258.96
15	SEG33	86.03	1580.74	66	XTALO	3464.94	2468.93
16	SEG32	86.03	1414.59	67	XTALI	3464.94	2588.98
17	SEG31	86.03	1249.93	68	RESETB	3464.94	2709.04
18	SEG30	86.03	1085.28	69	VSS	3464.94	2829.10
19	SEG29	86.03	920.63	70	PIOA7	3464.93	2949.13
20	SEG28	86.03	755.98	71	PIOA6	3464.93	3069.21
21	SEG27	86.03	591.33	72	PIOA5	3464.93	3187.51
22	SEG26	86.03	426.68	73	PIOA4	3464.93	3309.33
23	SEG25	86.03	262.03	74	NMIB	3464.94	3429.39
24	SEG24	131.00	86.03	75	EAB	3464.94	3554.97
25	SEG23	269.00	86.03	76	RI-CTL	3464.66	3680.59
26	SEG22	407.00	86.03	77	LED	3404.65	3819.01
27	SEG21	536.16	86.03	78	PIOA3	3279.09	3823.16
28	SEG20	657.60	86.03	79	PIOA2	3153.14	3823.16
29	SEG19	779.04	86.03	80	PIOA1	3033.06	3823.16
30	SEG18	900.48	86.03	81	PIOA0	2913.01	3823.16
31	SEG17	1021.92	86.03	82	VDD	2792.98	3823.11
32	SEG16	1143.36	86.03	83	PI7	2672.90	3823.11
33	SEG15	1264.80	86.03	84	PI6	2552.83	3823.11
34	SEG14	1386.24	86.03	85	PI5	2432.78	3823.11
35	SEG13	1507.68	86.03	86	PI4	2309.83	3823.11
36	SEG12	1629.12	86.03	87	PI3	2189.77	3823.11
37	SEG11	1750.56	86.03	88	PI2	2069.71	3823.11
38	SEG10	1872.00	86.03	89	PI1	1949.65	3823.11
39	SEG9	1993.44	86.03	90	PI0	1829.59	3823.11
40	SEG8	2113.50	86.03	91	PIOB5	1712.40	3823.11
41	SEG7	2233.56	86.03	92	PIOB4	1592.34	3823.11
42	SEG6	2353.62	86.03	93	PIOB3	1472.28	3823.11
43	SEG5	2473.68	86.03	94	PIOB2	1352.22	3823.11
44	SEG4	2593.74	86.03	95	PIOB1	1232.16	3823.11
45	SEG3	2713.80	86.03	96	PIOB0	1112.10	3823.11
46	SEG2	2833.85	86.03	97	OSCO	992.03	3823.11
47	SEG1	2953.93	86.03	98	OSCI	871.98	3823.11
48	COM16	3073.98	86.03	99	RXD	731.22	3823.11
49	COM15	3199.55	86.03	100	RTONE	576.66	3823.11
50	COM14	3325.13	86.03	101	DTONE	416.58	3823.11
51	COM13	3467.43	162.95	102	AVDD	258.74	3823.12

## Package Diagram



Symbol	Dimension in inch			Dimension in mm		
	Min	Type	Max	Min	Type	Max
<b>A</b>	—		0.134	—	—	3.40
<b>A1</b>	0.004	0.010	0.036	0.10	<b>0.25</b>	0.91
<b>A2</b>	0.102	0.112	0.122	2.60	<b>2.85</b>	3.10
<b>b</b>	0.005	0.009	0.013	0.12	<b>0.22</b>	0.32
<b>c</b>	0.002	0.006	0.010	0.05	<b>0.15</b>	0.25
<b>D</b>	0.541	0.551	0.561	13.75	<b>14.00</b>	14.25
<b>E</b>	0.778	0.787	0.797	19.75	<b>20.00</b>	20.25
<b>e</b>	0.010	0.020	0.030	0.25	<b>0.5</b>	0.75
<b>HD</b>	0.665	0.677	0.689	16.90	<b>17.20</b>	17.50
<b>HE</b>	0.902	0.913	0.925	22.90	<b>23.20</b>	23.50
<b>L</b>	0.027	0.035	0.043	0.68	<b>0.88</b>	1.08
<b>L1</b>	0.053	0.063	0.073	1.35	<b>1.60</b>	1.85
<b>y</b>	—	—	0.004	—	—	0.10
<b>θ</b>	0°	—	12°	0°	—	12°

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar rotrusion/intrusion.
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.

TITLE : 128 QFP (14x20 mm ) PACKAGE OUTLINE -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL :			
APPROVE		DOC. NO.	530-ASS-P004
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	Q128 - 1
		DATE	Apr. 1 1998
MSHINE Technologies Corporation			