Contents

Features

- 8-bit micro-controller built in
- **48K** bytes ROM (Read Only Memory)
- **2.8K** bytes RAM (Random Access Memory)
- Only single crystal (32768Hz)
- Programmable MCU clock rate
  High speed : 8.388MHz, 4.194MHz, 2.097MHz, 1.049MHz, 524KHz and **262KHz**.
  Low speed : 32768Hz.
- **MCU Power saving mode:**
  Clock rate = 524KHz, 262KHz and 32768Hz.
- DTMF generator & Frequency Shift Keying (FSK) Generator
- Ringer/Music tone generator
- Low voltage detector (**LVD**) / **Comparator**
- Programmable Low voltage reset (**LVR**)
- **Advance Power-On Reset** (Mask Option)
- Two 8-bit general-purposed timers
- A watchdog timer against deadlock.
- **UART** controller
- Universal synchronous serial Interface (**SSI**)
- Serial Memory Interface (**SMI2**)
- **MCCIN** interface with an additional 8-bit timer
- Auto Key scan function (1/8, 1/16 duty)
- **Seven-level** Priority-based interrupts.
- I/O ports and Multi-function I/O ports interface.
  - I/O port A: 8 pins general-purpose I/O ports with **Schmitt trigger interface**, and can interrupt independently.
  - I/O port B: **8** pins general-purpose I/O ports with non-open drain structure.
  - Open drain I/O port: **4** pins with heavy sinking capability. (PORT0~1, **MPORT0**, **PIOA7**)
  - Multiple-function I/O ports: **SEG33~40 (MPIOA)**, **COM1~8 (MPIOE)**, **COM9~12 (MPIOG), DTONE, VIN, RTIMB, MPORT0~7 with Schmitt trigger & interrupt.**
- Built-in LCD driver
  -Three programmable duties: 1/16, 1/8 or 1/4
  - Two programmable biases: 1/5, 1/4, or 1/3
  - Maximum 48 segment output pins
  - Maximum 16 common output pins
  - **32 level brightness adjustment**
- Power Management
  - Standby mode
  - Stop mode
  - Programmable internal PLL
- Operating voltage range: **2.5V~5.5V**

Block Diagram

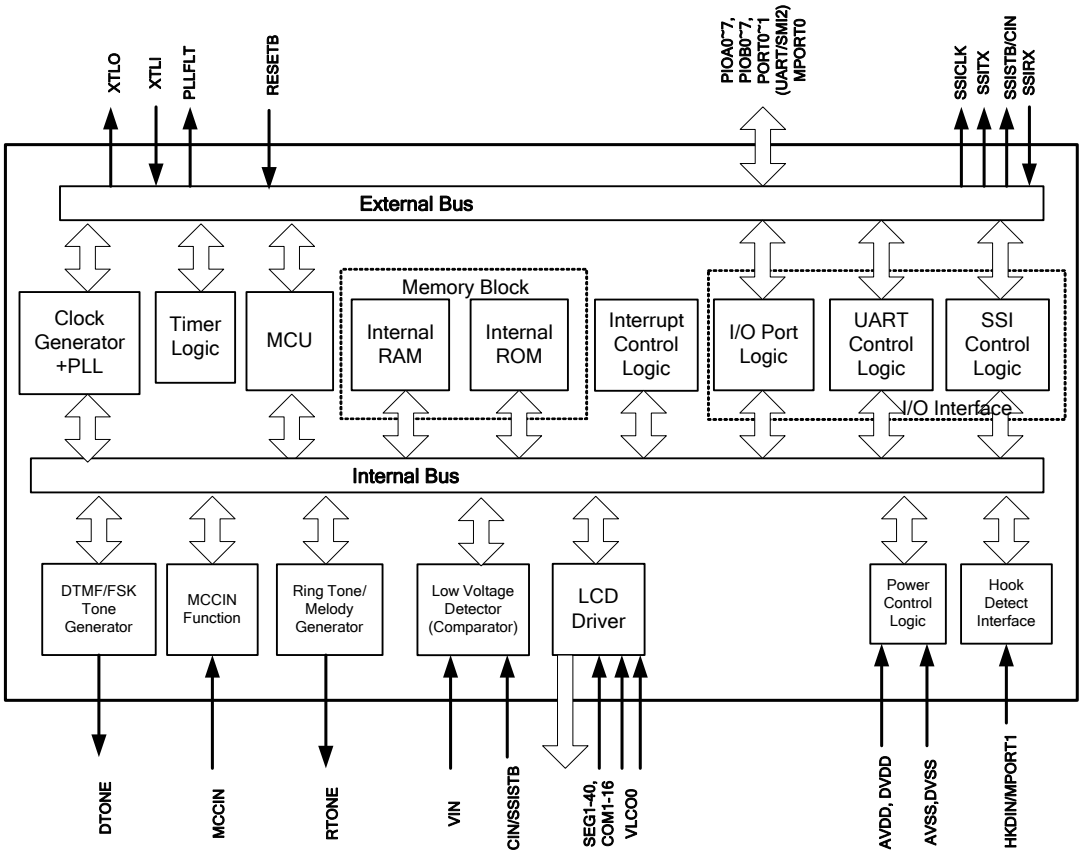


Figure 1, MS85065 Series Block Diagram.

Application

- Calculator

Package

- QFP100 packaged

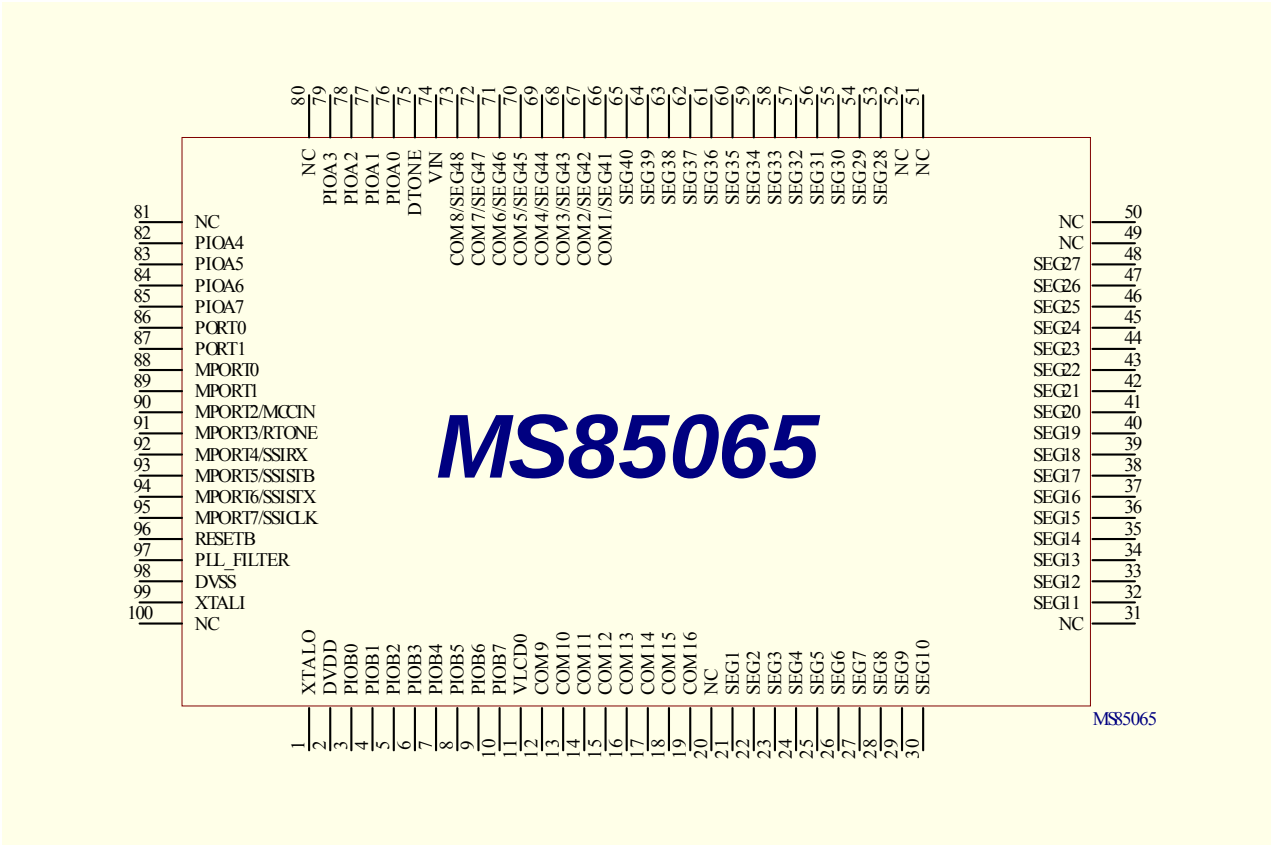
General Description

MS85065 are CMOS technology integrated circuits designed for the featured phone and calculator applications. A micro-controller is built-in to control the operation of the entire system. Two serial interfaces are used for the specified serial data transmission. Up to 32-degrees contrast levels are supported to adjust the LCD contrast. It also performs the power control to reduce the power dissipation. Moreover, the operating voltage is enhanced to **2.5V**. It provides a complete solution for the applications of the calculator, featured phones, and other communication systems.

Document Change History

2006/02/28: Version 1.

Pins Configuration



Pin Descriptions

Pin No.	Notation	I/O	Functional Description
2	DVDD	Power	Digital power supply input
98	DVSS	Power	Digital ground input.
96	RESETB	I	Reset pin of the chip. Active low. Schmitter trigger built in.
			Miscellaneous Interface`
74	VIN	I	Low-voltage detector input. (*see note 2)
93	**CIN (SSISTB)**	**I**	**Comparator input.**
			Oscillator & Clock Generator Interface
1	XTALO	O	32.768KHz oscillator output. A capacitor parallel connected to ground is required.
99	XTALI	I	32.768KHz oscillator input. A capacitor parallel connected to ground is required.
97	PLL_Filer	I	PLL Loop Filter Capacitor Pin. Connect to a resistor (typically R=1Kohm) and a capacitor(typically C=0.1uF)
			Telephone & Caller ID Interface
75	DTONE/FGTONE	O	DTMF/FSK signal output, or a programmable output pin. If tone-generator function is used, an external pull low 100K resistor is required.
			LCD Driver Interface
11	VLCD0	Power	LCD Driver Power Input.
21~30, 32~48, 53~65	SEG1–SEG40	O	Segment output pin for LCD driver. SEG**33~40** are multiple function pins and can be used for general-purposed I/O port. **The I/O port is named MPIOA. (SEG33~40 => MPIOA)**
66~73, 12~19	COM1–COM16	O	Common output pin for LCD driver. The COM9~16 pins are mainly used for the LCD driver. The **COM1~8** pins are multiple function pins either for the common of LCD driver or the general-purposed I/O port. The I/O port is named MPIOE. (COM1-8=> MPIOE). COM1~8 can also be switched to SEG41~48 at 1/8 duty or 1/4 duty mode.
			I/O Port Interface
76~79, 82~84	PIOA0–PIOA6	I/O	General-purposed I/O pins with internal pull-up resistors. These are **Schmitt trigger built in, and readable.** These can also be programmed as **auto key scanning** input pins.
85	PIOA7	I/O	General-purposed I/O pins with open-drain output. Note that the open-drained output has no internal pull-high resistor.
3~10	PIOB0–PIOB**7**	I/O	General-purposed I/O pins with internal pull-up resistors, which can also be programmed as **auto key scanning** input pins.
86,86	PORT0~1	I/O	General-purposed I/O pins with open-drain and heavy sinking structure. (max 10mA). PORT{0~1} are also multiple-function pins with SMI2/UART interface.
88	MPORT0	I/O	General-purposed I/O pins with open-drain output & interrupt function.
			Peripheral Interface
95	MPORT7/SSICLK	I/0	This pin is multiple-function pin. It can be used either for SSI clock pin or for GPIO pin. As SSI interface and master, this pin is input with Schmitt trigger.
94	MPORT6/SSITX	I/0	This pin is multiple-function pin. It can be used either for SSI TX pin or for GPIO pin. As SSI interface and slave, this pin is Hi-Z in idle state (SSISTB enabled)
93	MPORT5/SSISTB	I/0	This pin is multiple-function pin. It can be used either for SSI strobe pin or for GPIO pin. As SSI interface and slave, this pin can be used for SSI module enable pin.
92	MPORT4/SSIRX	I/0	This pin is multiple-function pin. It can be used either for SSI RX pin or for GPIO pin. As SSI interface, this pin is Hi-Z in idle state. (no SSICLK input)
91	MPORT3/RTONE	I/O	This pin is multiple-function pin. It can be used either for clock wave output or GPIO pin.

90	MPORT2/MCCIN	I/0	This pin is multiple-function pin. It can be used either for MCC module input pin or for GPIO pin. This pin is Schmitt trigger input pin. For MCCIN, this pin is used to measure the pulse length of square wave.
89	**MPORT1**	I/0	This pin is a GPIO pin with interrupt capability.

Absolute Maximum Ratings

Comments

DC Supply Voltage.....-0.5V to + 5.5V
Input Voltage……..-0.5V to VDD + 0.5V
Output Voltage……-0.5V to VDD + 0.5V
Operating Temperature….....0° to 70° C
Storage Temperature……..-40° to 150° C

Never allow a stress to exceed the values listed under "Absolute Maximum Ratings", otherwise the device would suffer from a permanent damage. Nor is a stress at the listed value be allowed to persist over a period, since an extended exposure to the absolute maximum rating condition may also affect the reliability of the device, if not causing a damage thereof.

AC & DC Electrical Characteristics

DC Electrical Characteristics (Temperature=0°C to 70°C, V_{DD}=4.5V, GND=0V)

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	MCU operating voltage	V_{DD}	2.2	3.6	5.5	V
	DTMF, Ring Tone Generator	$V_{DTMF,RING}$	2.2	3.6	5.5	V
Supply Current	ROM operating voltage (<=4.19MHz)	V_{ROML}	2.2	3.6	5.5	V
	ROM operating voltage (8.38MHz)	V_{ROMH}	2.8	3.6	5.5	V
	RAM operating voltage	V_{RAM}	2.0	3.6	5.5	V
	Current Consumption of Low Speed MCU Mode (PLL off, 32.768KHz on, DTMF off, LCD on)	I_{LSP}	-	100		μA
	Current Consumption of Standby Mode (PLL on, 32.768KHz on, DTMF off, LCD off)	I_{PLL}	-	**100**	-	μA
	Current Consumption of Standby Mode (MCU off, PLL off, 32.768KHz on, DTMF off, LCD off)	I_{STDY}	-	**10**	-	μA
	Current Consumption of Stop Mode (MCU off, PLL off, 32.768KHz off, DTMF off, LCD off)	jI_{STOP}	-	3	5[1]	μA
Output voltage	I_{OH}=1 mA , PIOA, PIOB, MPA~D, MPORT, and PORT0~1 pins	V_{OH1}	VDD-0.2	-	-	V
	I_{OL}=2 mA, PIOA, PIOB, MPA~D, MPORT, and PORT0~1 pins	V_{OL1}	0.2	-	-	V
	I_{OL}=2.2 mA, PORT0~1 open-drained	V_{OL2}	0.2	-	-	V
Input voltage	PIOA, PIOB, MPA~D, MPORT, and PORT0~1 pins	V_{IH1}	0.8 V_{DD}	-	V_{DD}+0.3	V
	PIOA, PIOB, MPA~D, MPORT, and PORT0~1 pins	V_{IL1}	-0.3	-	0.2 V_{DD}	V
Output current	V_{OH}=4.0V, PIOA, PIOB, MPA~D, MPORT, and PORT0~1 pins V_{OH}=3.6V	I_{OH1}		3		mA
	V_{OH}=0.9V, PIOA and PIOB pins V_{OH}=0.5V	I_{OL1}		15 8		mA
	V_{OH}=0.9V, Port 0~1 open-drained V_{OH}=0.5V	I_{OL2}		15 8		mA
Pull-up resistor	MPA~D, MPORT, and PORT0~1	R_{PULL}	-	100	-	KΩ
	PIOA, PIOB, selected by s/w	$R_{A,B,PULL}$	100		600	KΩ

[1] The leakage is from the “power on reset” (APOR) circuits of MS85065.

AC Electrical Characteristics – Internal Phase Lock Loop (Temperature=0°C to 70°C, V_{DD}=3.0V, GND=0V)

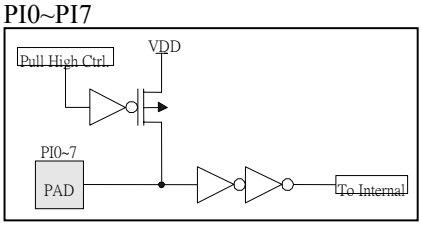
Parameters	Min.	Typ.	Max.	Unit
Main Frequency	-	8388608	-	Hz
PLL Lock Time	-	5.0	-	ms

AC Electrical Characteristics – DTMF Generator (Temperature=0°C to 70°C, V_{DD}=3.3V, GND=0V)

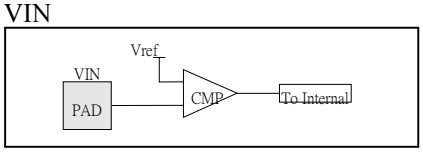
Parameters	Min.	Typ.	Max.	Unit
Frequency Deviation	-	-	0.6%	
Total Harmonic Distortion (THD)	-	-	4%	
High Frequency Output AC Level	-	364	-	mV_{pp}
Low Frequency Output AC Level	-	284	-	mV_{pp}
Signal Twist		2.18		DB

Appendix A. Pins Configuration

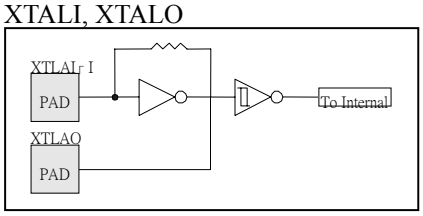
PI0~PI7



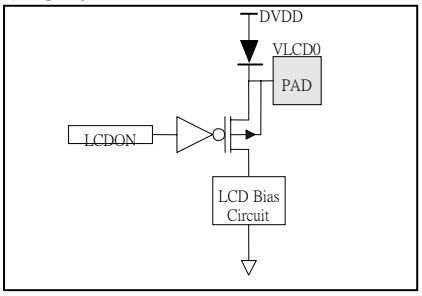
VIN



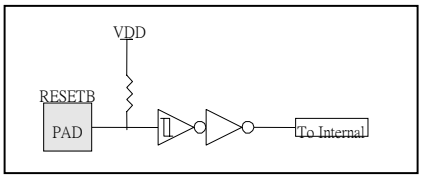
XTALI, XTALO



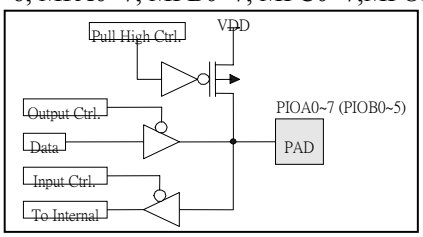
VLCD0



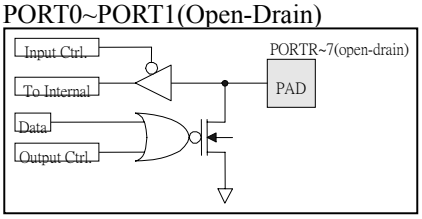
RESETB



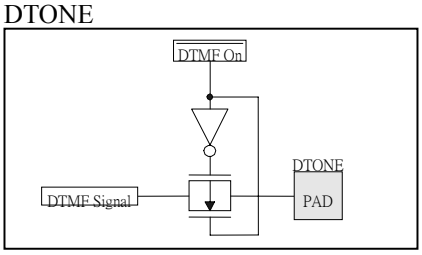
PIOA0~6, MPA0~7, MPB0~7, MPC0~7,MPORT0~7(for I/O)



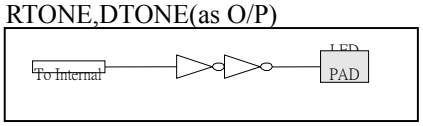
PORT0~PORT1(Open-Drain)



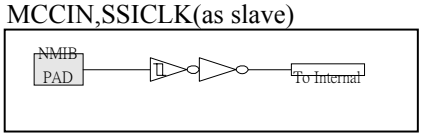
DTONE



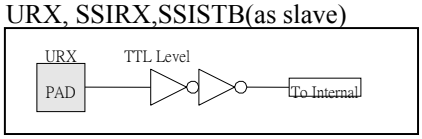
RTONE,DTONE(as O/P)



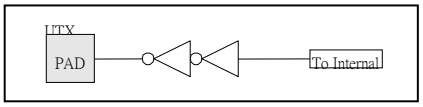
MCCIN,SSICLK(as slave)



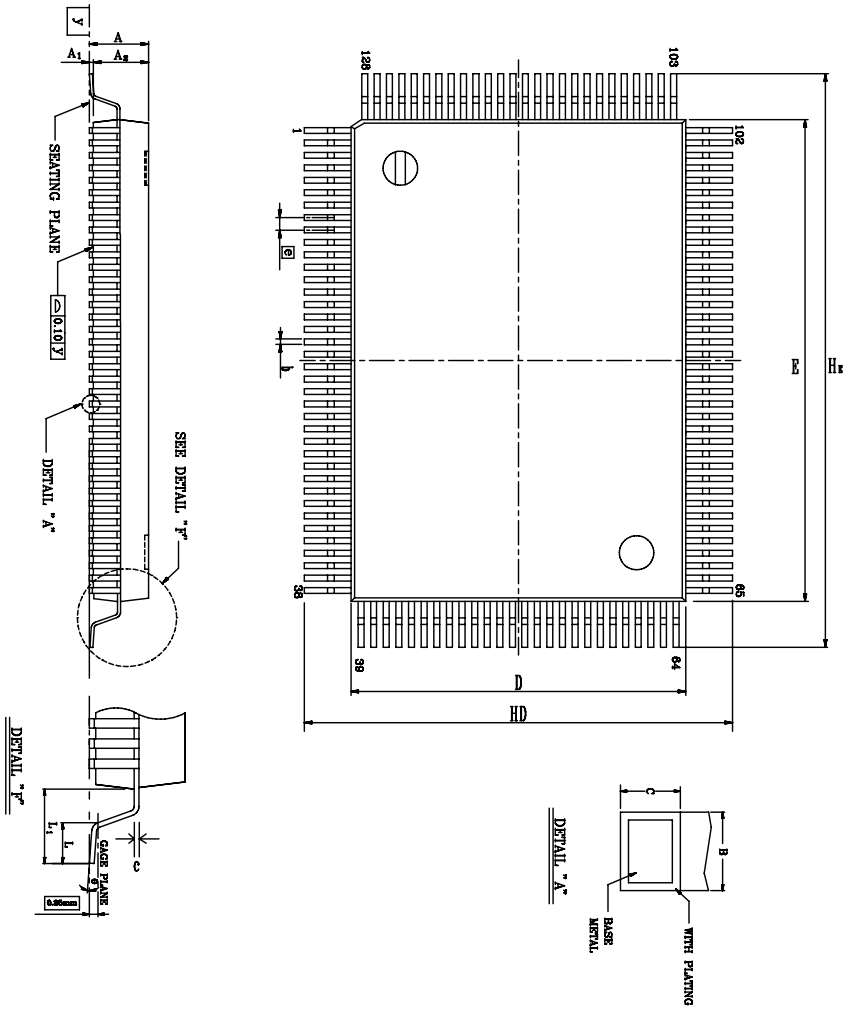
URX, SSIRX,SSISTB(as slave)



UTX, SSICLK(as master), SSITX, SSISTB(as mater)



Appendix B. Package Diagram



Symbol	Dimension in inch			Dimension in mm		
	Min	Type	Max	Min	Type	Max
A	—		0.134	—	—	3.40
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.102	0.112	0.122	2.60	**2.85**	3.10
b	0.005	0.009	0.013	0.12	**0.22**	0.32
c	0.002	0.006	0.010	0.05	**0.15**	0.25
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e	0.010	0.020	0.030	0.25	**0.5**	0.75
HD	0.665	0.677	0.689	16.90	**17.20**	17.50
HE	0.902	0.913	0.925	22.90	**23.20**	23.50
L	0.027	0.035	0.043	0.68	**0.88**	1.08
L1	0.053	0.063	0.073	1.35	**1.60**	1.85
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

Note :

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar rotrusion/intrusion.
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.

TITLE : **128 QFP** (14x20 mm) PACKAGE OUTLINE -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL :			
APPROVE		DOC. NO.	530-ASS-P004
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	Q128 - 1
		DATE	Apr. 1 1998
MSHINE Technologies CO., LTD			