MS8506CP/MS85066 Datasheet

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Features

- 8-bit micro-controller built in
- **48K** bytes ROM (Read Only Memory)
- **2.8K** bytes RAM (Random Access Memory)
- Only single crystal (32768Hz)
- Programmable MCU clock rate
  High speed : 8.388MHz, 4.194MHz, 2.097MHz, 1.049MHz, 524KHz and **262KHz**.
  Low speed : 32768Hz.
- **MCU Power saving mode:**
  Clock rate = 524KHz, 262KHz and 32768Hz.
- Frequency Shift Keying (FSK) Transceiver & Carrier detector
- CAS (CPE Alert Signal)/TAS detector
- **Programmable** DTMF generator (**New Scheme**)
- **DTMF Detector**
- **Dual mode detector (FSK and DTMF)**
- **Stuttered Dial Tone (SDT) detector**
- Ring and line reversal detector
- Ringer/Music tone generator
- Low voltage detector (**LVD**) / **Comparator**
- Programmable Low voltage reset (**LVR**)
- **Advance Power-On Reset** (Mask Option)
- **No Ring Detector (NRD)**
- Two 8-bit general-purposed timers
- A watchdog timer against deadlock.
- **UART** controller
- Universal synchronous serial Interface (**SSI**)
- Serial Memory Interface (**SMI2**)
- **MCCIN** interface
- **Hook Detect Interface**
- Auto Key scan function (1/8, 1/16 duty)
- **Seven-level** Priority-based interrupts.
- I/O ports and Multi-function I/O ports interface.
  - I/O port A: 8 pins general-purpose I/O ports with **Schmitt trigger interface**, and can interrupt independently.
  - I/O port B: **8** pins general-purpose I/O ports with non-open drain structure.
  - Open drain I/O port: **4** pins with heavy sinking capability. (PORT0~1, **MPORT0**, **PIOA7**)
  - Multiple-function I/O ports: **SEG33~40 (MPIOA)**, **COM1~8 (MPIOE)**, **DTONE, CASIN, VIN, RTIMB, MPORT0~7 with Schmitt trigger & interrupt.**
- Built-in LCD driver
  -Three programmable duties: 1/16, 1/8 or 1/4
  - Programmable biases: 1/3, 1/5 or 1/4
  - Maximum 48 segment output pins[1]
  - Maximum 16 common output pins
  - **32 level brightness adjustment**
- Power Management
  - Standby mode
  - Stop mode
  - Programmable internal PLL
- Operating voltage range: **2.5V~5.5V**

[1] MS8506CP supports 8x48, 16x40, but not 16x48.
MS85066 supports 16x48, 16x40,8x48, and 8x40.

Block Diagram

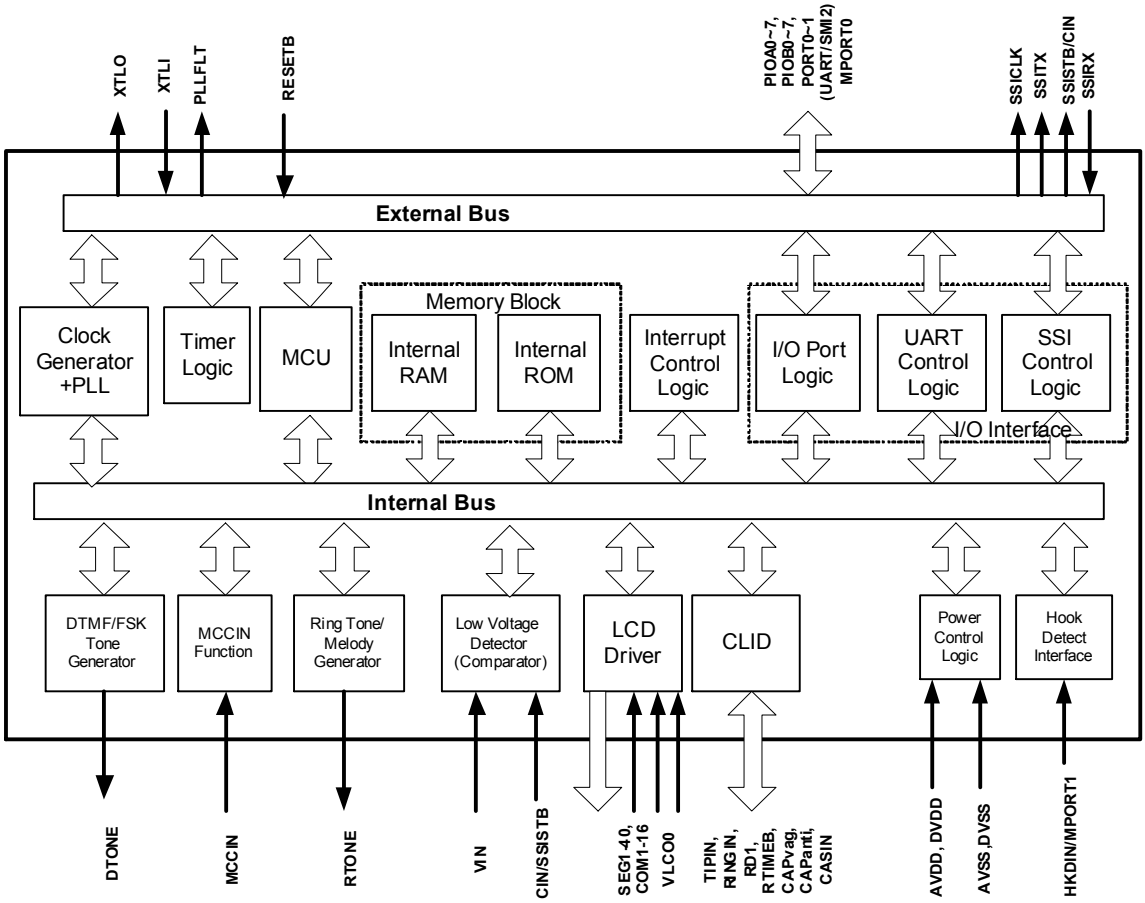


Figure 1, MS8506 Series Block Diagram.

Application

- Calling number delivery (CND) &
  Calling name delivery (CNAM) features
- Caller identification on call waiting (CIDCW) features
- Corded or Cordless adjunct boxes phone set
- Short Message Service (SMS) system
- Corded or Cordless Feature phones
- Other communication systems

Package

- QFP128 packaged

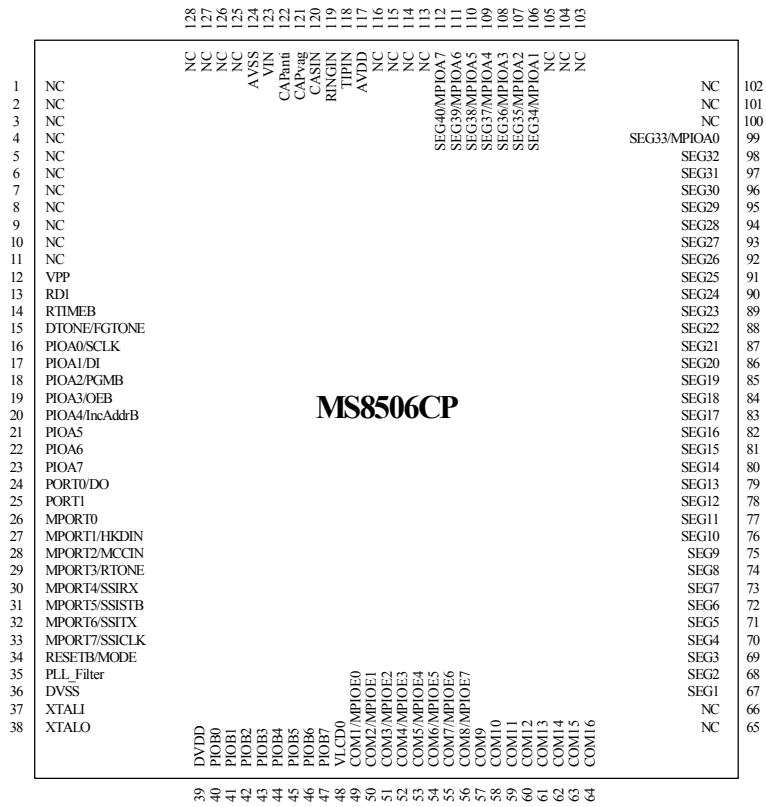
General Description

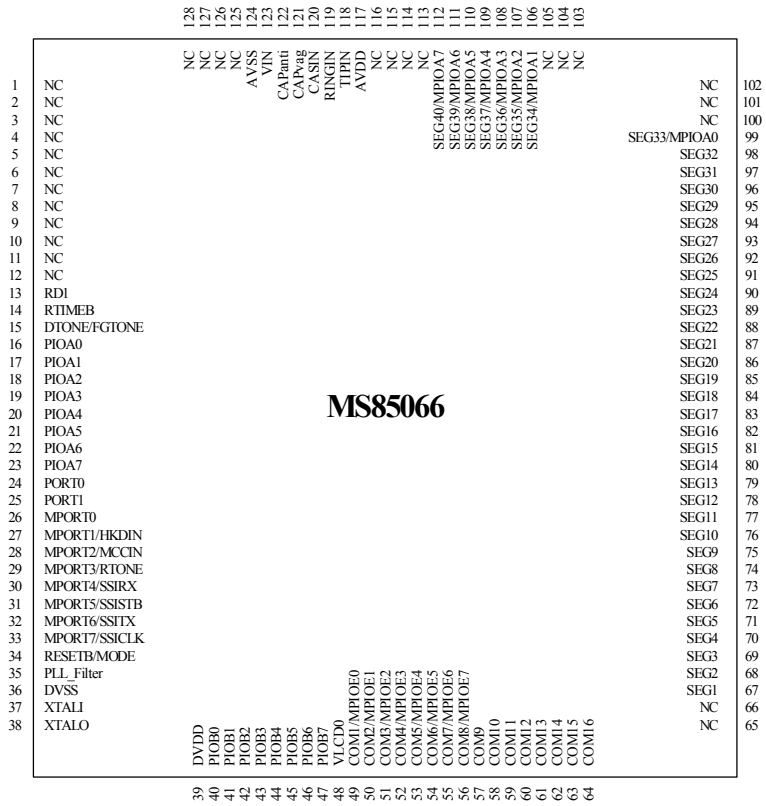
The MS85066 series are CMOS technology integrated circuits designed for the corded/cordless phone applications with the caller ID functions. A micro-controller is built-in to control the operation of the entire system. The MS8506 series fulfills all the features and functions offered by the former series product, also including the functionalities of FSK transceiver, a high performance CPE Alerting Tone (CAS) detection, DTMF generation and decoder, Ring detection and Low Voltage indication. There are several I/O interfaces designed for handshaking with the other peripheral devices. The I/O ports are used for the general-purpose application. Two serial interfaces are used for the specified serial data transmission. Up to 32-degrees contrast levels are supported to adjust the LCD contrast. It also performs the power control to reduce the power dissipation. Moreover, the operating voltage is enhanced to **2.5V**. It provides a complete solution for the applications of the adjunct boxes, feature phones, and other communication systems.

Document Change History

2003/12/11 First release (Ver:0.1)
2003/12/12: (Ver: 0.2) ➔ Add CASGC2 control register to control register mapping table.
2003/12/12: (Ver: 0.3) ➔ Modified control register “TGMC” of DTMF generator.
2003/12/19: (Ver: 0.4) ➔ Modified NRD, Interrupt, DTMF Gen., Control Reg. & Pins Config.
➔ Add one pin “CAPanti”.
2004/01/06: (Ver: 0.5) ➔ Modified address of “DIVAL1” & “DIVAL2”.
2004/02/02: (Ver: 0.6) ➔ Modified PIOA7 & MPORT0 to be open-drain pins when as output port.
2004/02/03: (Ver: 0.7) ➔ Modified description of SSI chapter.
2004/03/18: (Ver: 0.8) ➔ Add MS8506P Bonding Diagram.
2004/04/05: (Ver:0.91) ➔ Add NRD ON/OFF flag.
2004/05/12: (Ver:0.92) ➔ Modify MS8506P Bonding Diagram and Pin Configuration. (OTP Pin)
2004/06/16: (Ver:0.94) ➔ Add 2 open drained pins PIOA7 & MPORT0, and more applications notes about SMI, etc.
2004/06/21: (Ver:0.96) ➔ Note about CID bits changing, ring, contents, and Index.
2004/09/20: (Ver:0.97) ➔ ADD LVR/LVD/NRD modification.

Pins Configuration





Pin Descriptions

Pin No.	Notation	I/O	Functional Description
117	AVDD	Power	Analog power supply Input.
124	AVSS	Power	Analog ground input.
39	DVDD	Power	Digital power supply input
36	DVSS	Power	Digital ground input.
34	RESETB	I	Reset pin of the chip. Active low. Schmitter trigger built in.
			Miscellaneous Interface`
123	VIN	I	Low-voltage detector input. (*see note 2)
31	**CIN (SSISTB)**	**I**	**Comparator input.**
			Oscillator & Clock Generator Interface
38	XTALO	O	32.768KHz oscillator output. A capacitor parallel connected to ground is required.
37	XTALI	I	32.768KHz oscillator input. A capacitor parallel connected to ground is required.
35	PLL_Filer	I	PLL Loop Filter Capacitor Pin. Connect to a resistor (typically R=1Kohm) and a capacitor(typically C=0.1uF)
			Telephone & Caller ID Interface
118	TIPIN	I	This input pin is connected to the tip side of the twisted pair line. FSK signal or CAS signal can be delivered into this pin. (*See note 1)
119	RINGIN	I	This input pin is connected to the ring detector input of the twisted pair line. (*See note 1)
120	CASIN	I	This is a single-ending input pin for CAS signal detection, alternatively used different from TIPIN/RINGIN. Usually this pin is connected to side-tone cancelled signal from the speech network circuits. Internal programmable amplifier can recover back the attenuation caused by the speech network.
13	RD1	I	Ring Detector Input pin. This pin is normally coupled to the one of the twisted pair wires through an attenuating network. While no ring coming, this pin should be low state. With AC coupled from the phone line, logic high comes at this pin. Please check “Ring Detector” section for details.
14	RTIMEB	I	Ring time control signal input pin or general-purpose input pin. It is necessary to apply a proper RC circuit with a specified time constant for examine the validation of ring signal. Please check “Ring Detector” section for details.
15	DTONE/FGTONE	O	DTMF/FSK signal output, or a programmable output pin. If tone-generator function is used, an external pull low 100K resistor is required.
121	**CAPvag**	**I**	Connect to external capacitor (typical: 0.5uF)
122	**CAPanti**	**I**	Connect to external Capacitor for anti-aliasing filter (typical: 1nF)
			LCD Driver Interface
48	VLCD0	Power	LCD Driver Power Input.
67~99, 106~112	SEG1–SEG40	O	Segment output pin for LCD driver. SEG**33~40** are multiple function pins and can be used for general-purposed I/O port. The I/O port is named MPIOA. (SEG33~40 => MPIOA)
49~64	COM1–COM16	O	Common output pin for LCD driver. The COM9~16 pins are mainly used for the LCD driver. The **COM1~8** pins are multiple function pins either for the common of LCD driver or the general-purposed I/O port. The I/O port is named MPIOE. (COM1-8=> MPIOE).
			I/O Port Interface
16~22	PIOA0–PIOA6	I/O	General-purposed I/O pins with internal pull-up resistors. These are **Schmitt trigger built in, and readable.** These can also be programmed as **auto key scanning** input pins.

23	PIOA7	I/O	General-purposed I/O pins with open-drain output. Note that the open-drained output has no internal pull-high resistor.

40~47	PIOB0–PIOB7	I/O	General-purposed I/O pins with internal pull-up resistors, which can also be programmed as **auto key scanning** input pins. For 16x48 LCD resolution, PIOB0~7 will act as LCD segment 41~48.
24,25	PORT0~1	I/O	General-purposed I/O pins with open-drain and heavy sinking structure. (max 10mA). PORT{0~1} are also multiple-function pins with **SMI2/UART** interface.
26	MPORT0	I/O	General-purposed I/O pins with open-drain output & interrupt function.
Peripheral Interface			
33	MPORT7/SSICLK	I/0	This pin is multiple-function pin. It can be used either for SSI clock pin or for GPIO pin. As SSI interface and master, this pin is input with Schmitt trigger.
32	MPORT6/SSITX	I/0	This pin is multiple-function pin. It can be used either for SSI TX pin or for GPIO pin. As SSI interface and slave, this pin is Hi-Z in idle state (SSISTB enabled)
31	MPORT5/SSISTB	I/0	This pin is multiple-function pin. It can be used either for SSI strobe pin or for GPIO pin. As SSI interface and slave, this pin can be used for SSI module enable pin.
30	MPORT4/SSIRX	I/0	This pin is multiple-function pin. It can be used either for SSI RX pin or for GPIO pin. As SSI interface, this pin is Hi-Z in idle state. (no SSICLK input)
29	MPORT3/RTONE	I/O	This pin is multiple-function pin. It can be used either for clock wave output or GPIO pin.
28	MPORT2/MCCIN	I/0	This pin is multiple-function pin. It can be used either for MCC module input pin or for GPIO pin. This pin is Schmitt trigger input pin. For MCCIN, this pin is used to measure the pulse length of square wave.
27	**MPORT1/HKDIN**	I/0	This pin is multiple-function pin. It can be used either for **Hook Detect Interface** input pin or for GPIO pin.
OTP Function Pins (FOR MS8506P Only)			
12	**VPP**	Power	This pin is for OTP programming voltage source.
34	**MODE/RESETB**	I	When RESETB is low, MS8506P is in OTP Mode.
16	**PIOA0/SCLK**	I	Input Programming clock when in OTP Mode.
17	**PIOA1/DI**	I	Input Data when in OTP Mode.
18	**PIOA2/PGMB**	I	Low indicates to “program” the OTP ROM.
19	**PIOA3/OEB**	I	Low will output compare OK to DO.
20	**PIOA4/IncADDRB**	I	Low pulse will increase internal address counter.
24	**PORT0/DO**	O	Output of compare result.

Note 1: ‘TIPIN’ and ‘RINGIN’ must be DC isolated from the phone line.
Note 2: The detected voltage level can be adjusted by using an external voltage divider circuit.
Note 3: It is suggested that the power pins AVDD and DVDD are blocked by coil for de-coupling the noise from analog circuit to digital circuit. (AVSS and DVSS, too)
Note 4: To avoid the problem of line unbalance, the ground of any test machine, such as oscilloscope or AI, must be isolated from the ground of this chip.

Absolute Maximum Ratings

Comments

DC Supply Voltage.....-0.5V to + 6.0V
Input Voltage……..-0.5V to VDD + 0.5V
Output Voltage……-0.5V to VDD + 0.5V
Operating Temperature…....0° to 70° C
Storage Temperature……..-40° to 150° C

Never allow a stress to exceed the values listed under "Absolute Maximum Ratings", otherwise the device would suffer from a permanent damage. Nor is a stress at the listed value be allowed to persist over a period, since an extended exposure to the absolute maximum rating condition may also affect the reliability of the device, if not causing a damage thereof.

AC & DC Electrical Characteristics

DC Electrical Characteristics (Temperature=0°C to 70°C, V_{DD}=4.5V, GND=0V)

Parameters	Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	MCU operating voltage	V_{DD}	2.2	3.6	5.5	V
	FSK operating voltage	V_{DDF}	**2.5**	3.6	5.5	V
	CAS operating voltage	V_{DDC}	**2.5**	3.6	5.5	V
	DTMF, Ring Tone Generator	$V_{DTMF,RING}$	2.2	3.6	5.5	V
	ROM operating voltage (<=4.19MHz)	V_{ROML}	2.2	3.6	5.5	V
	ROM operating voltage (8.38MHz)	V_{ROMH}	2.8	3.6	5.5	V
	RAM operating voltage	V_{RAM}	2.0	3.6	5.5	V
Supply current	FSK/CAS/DTMF demodulator Current Consumption **(3.6V)**	I_{FSK}	-	**2.0**	mA	
	FSK/DTMF Generator Current Consumption	I_{DTMF}	-	**1.6**	mA	
	Current Consumption of Low Speed MCU Mode (PLL off, 32.768KHz on, CAS off, FSK off, DTMF off, LCD on)	I_{LSP}	-	100		µA
	Current Consumption of Standby Mode (PLL on, 32.768KHz on, CAS off, FSK off, DTMF off, LCD off)	I_{PLL}	-	**100**	-	µA
	Current Consumption of Standby Mode (MCU off, PLL off, 32.768KHz on, CAS off, FSK off, DTMF off, LCD off)	I_{STDY}	-	**10**	-	µA
	Current Consumption of Stop Mode (MCU off, PLL off, 32.768KHz off, CAS off, FSK off, DTMF off, LCD off)	jI_{STOP}	-	3	5[2]	µA
Output voltage	I_{OH}=1 mA , PIOA, PIOB, MPA~D, MPORT, and PORT0~1 pins	V_{OH1}	VDD-0.2	-	-	V
	I_{OL}=2 mA, PIOA, PIOB, MPA~D, MPORT, and PORT0~1 pins	V_{OL1}	0.2	-	-	V
	I_{OL}=2.2 mA, PORT0~1 open-drained	V_{OL2}	0.2	-	-	V
Input voltage	PIOA, PIOB, MPA~D, MPORT, and PORT0~1 pins	V_{IH1}	0.8 V_{DD}	-	V_{DD}+0.3	V
	PIOA, PIOB, MPA~D, MPORT, and PORT0~1 pins	V_{IL1}	-0.3	-	0.2 V_{DD}	V
Output current	V_{OH}=4.0V, PIOA, PIOB, MPA~D, MPORT, and PORT0~1 pins V_{OH}=3.6V	I_{OH1}		3		mA
	V_{OH}=0.9V, PIOA and PIOB pins V_{OH}=0.5V	I_{OL1}		15 8		mA
	V_{OH}=0.9V, Port 0~1 open-drained V_{OH}=0.5V	I_{OL2}		15 8		mA
Pull-up resistor	MPA~D, MPORT, and PORT0~1	R_{PULL}	-	100	-	KΩ
	PIOA, PIOB, selected by s/w	$R_{A,B,PULL}$	100		600	KΩ

[2] The leakage is from the “power on reset” (APOR) circuits of MS8506P.

AC Electrical Characteristics – FSK Demodulation (Temperature=0°C to 70°C, V_{DD}=3.6V, GND=0V) [CPE refer to open loop, not 600ohms test load]

Parameters	Conditions	Min.	Typ.	Max.	Unit
Input sensitivity of Tip and Ring	S/N=25, Baud rate=1200 Bps Mark=1200Hz, Space=2200Hz	-	-48	-	dBm
SNR of input signal	Signal level = 0~-45dBm Baud rate=1200 Bps Mark=1200Hz, Space=2200Hz	-	13	-	dB
Baud Rate	Signal level = -45dBm, S/N=25 Mark=1200Hz, Space=2200Hz	1150	1200	1250	Bps
Positive twist (twist = mark signal level-space signal level) Negative twist	Signal level=-45dBm, S/N=25, Baud rate=1200Bps	-	+12 -8	-	dB
Bell 202 FSK Mark frequency Space frequency	Signal level=-45dBm, S/N=25 Baud rate=1200Bps	1100 2100	1200 2200	1300 2300	Hz
V.23 FSK Mark frequency Space frequency	Signal level=-45dBm, S/N=25 Baud rate=1200Bps	1200 2100	1300 2200	1400 2300	Hz
Bandpass Frequency Response (TBD)	60Hz 100Hz 400Hz 1200Hz 2200Hz 2700Hz 3500Hz 4000Hz	-	-25.0 -25.0 -12.0 0 0 -2.1 -6 -20	-	dB

AC Electrical Characteristics – DTMF Detector (Temperature=0°C to 70°C, V_{DD}=3.6V, GND=0V) [CPE interface with 600ohms test load] (TBD)

Parameters	Conditions	Min.	Typ.	Max.	Unit
Input sensitivity of Tip and Ring (Dual tone)	S/N=25, Frequency deviation=0%	-34	-	+1	dBm
Input Signal Reject Level (Dual tone)	S/N=25, Frequency deviation=0%	-40		-	dBm
SNR of input signal	Third Tone Noise Tolerance	-	18	-	dB
	AWGN Noise Tolerance	-	15	-	
Signal Twist (twist = high tone signal level –low tone signal level)	Signal level=-25dBm, S/N=25, Frequency deviation<1.5%	-	+8 +8	-	dB
Frequency Deviation	Signal level=-25dBm, S/N=25	±2%			Hz
Signal Duration tolerance	Signal level=-25dBm, S/N=25 Frequency deviation<1.5%	40ms/40ms ON/OFF time (Typically)			Hz

AC Electrical Characteristics – CAS Detection (Temperature=0°C to 70°C, V_{DD}=3.6V, GND=0V) [CPE refer to 600ohms test load]

Parameters	Conditions	Min.	Typ.	Max.	Unit
CAS Signal Sensitivity	CAS=2130Hz,2750Hz ,twist=0db ,Duration=80ms, no speech mode.	-37 (per tone)	-22 (per tone)	0	dBm
TAS Signal Sensitivity	CAS=2130Hz,2750Hz, twist=0db,Duration=80ms, no speech mode.	-42 (per tone)	-22 (per tone)	0	
Frequency Deviation	twist=0db,Duration=80ms, no speech mode.		2130+/- 2% 2750+/- 2%		Hz
Tone Duration	CAS=2130Hz,2750Hz ,twist=0db, no speech mode.	65	-	125	ms
Signal reject level		-	-46	-	dBm

CPT/SDT Detector Signal Parameter. (TBD) [CPE interface with 600ohms test load]

Parameters	Conditions	Min.	Typ.	Max.	Unit
Input sensitivity of Tip and Ring (Dual tone)	S/N=25, Frequency deviation=0%	-40	-	-2	dBm
Input Signal Reject Level (Dual tone)	S/N=25, Frequency deviation=0%	-46		-	dBm
SNR of input signal	Third Tone Noise Tolerance	-	18	-	dB
	AWGN Noise Tolerance	-	15	-	
Signal Twist (twist = high tone signal level –low tone signal level)	Signal level=-25dBm, S/N=25, Frequency deviation<1.5%	-	+8 +8	-	dB
Frequency Deviation	Signal level=-25dBm, S/N=25	±2%			Hz
Signal Duration tolerance	Signal level=-25dBm, S/N=25 Frequency deviation<1.5%	40ms/40ms ON/OFF time (Typically)			Hz

AC Electrical Characteristics – Internal Phase Lock Loop (Temperature=0°C to 70°C, V_{DD}=4.5V, GND=0V)

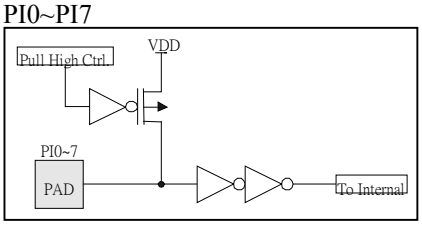
Parameters	Min.	Typ.	Max.	Unit
Main Frequency	-	8388608	-	Hz
PLL Lock Time	-	5.0	-	ms

AC Electrical Characteristics – DTMF Generator (Temperature=0°C to 70°C, V_{DD}=4.5V, GND=0V)

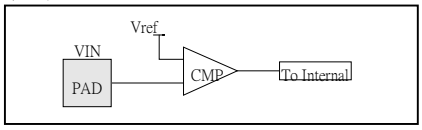
Parameters	Min.	Typ.	Max.	Unit
Frequency Deviation	-	-	0.6%	
Total Harmonic Distortion (THD)	-	-	4%	
High Frequency Output AC Level	-	364	-	mV_{pp}
Low Frequency Output AC Level	-	284	-	mV_{pp}
Signal Twist		2.18		DB

Appendix A. Pins Configuration

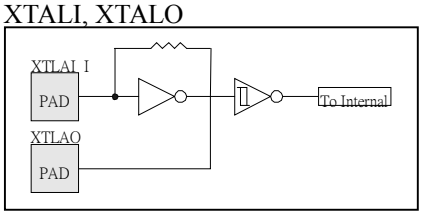
PI0~PI7



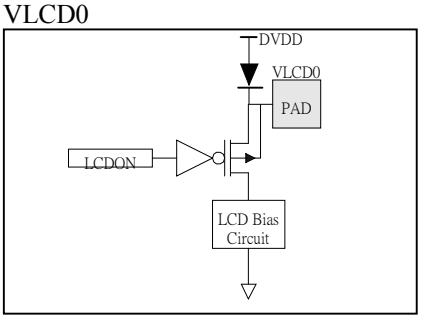
VIN



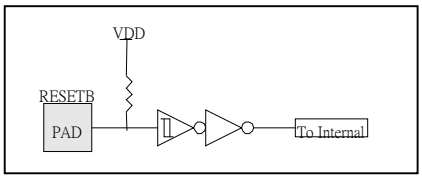
XTALI, XTALO



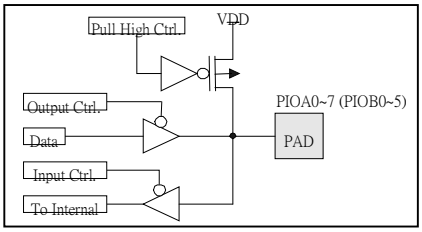
VLCD0



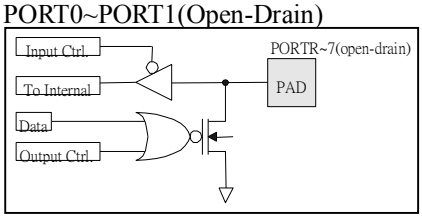
RESETB



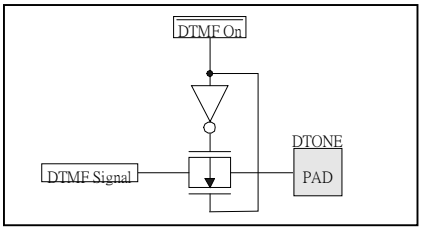
PIOA0~6, MPA0~7, MPB0~7, MPC0~7,MPORT0~7(for I/O)



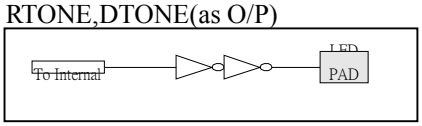
PORT0~PORT1(Open-Drain)



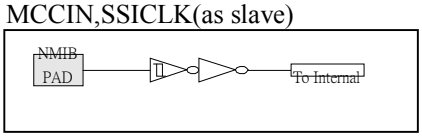
DTONE



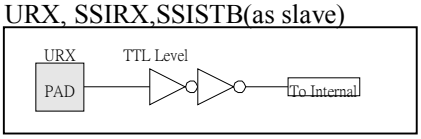
RTONE,DTONE(as O/P)



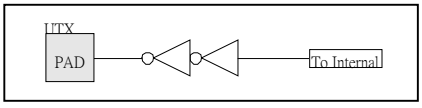
MCCIN,SSICLK(as slave)



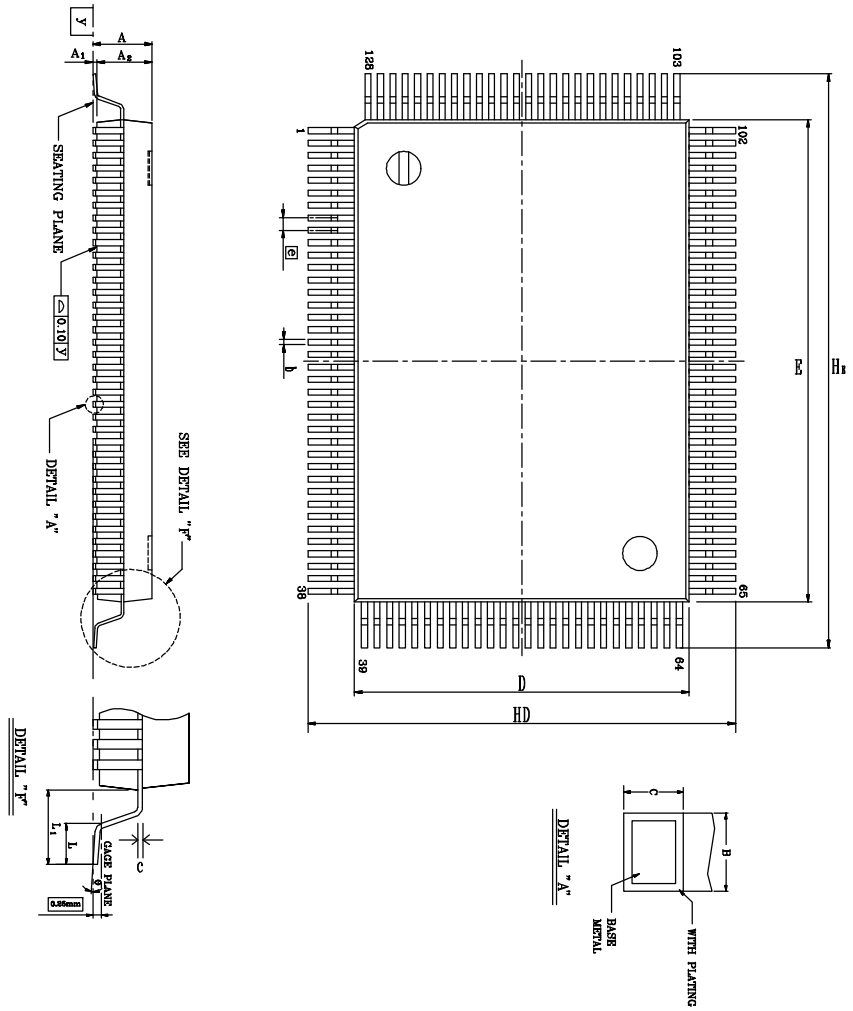
URX, SSIRX,SSISTB(as slave)



UTX, SSICLK(as master), SSITX, SSISTB(as mater)



Appendix B. Package Diagram



Symbol	Dimension in inch			Dimension in mm		
	Min	Type	Max	Min	Type	Max
A	—		0.134	—	—	3.40
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.102	0.112	0.122	2.60	**2.85**	3.10
b	0.005	0.009	0.013	0.12	**0.22**	0.32
c	0.002	0.006	0.010	0.05	**0.15**	0.25
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e	0.010	0.020	0.030	0.25	**0.5**	0.75
HD	0.665	0.677	0.689	16.90	**17.20**	17.50
HE	0.902	0.913	0.925	22.90	**23.20**	23.50
L	0.027	0.035	0.043	0.68	**0.88**	1.08
L1	0.053	0.063	0.073	1.35	**1.60**	1.85
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

Note :

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar rotrusion/intrusion.
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.

TITLE : **128 QFP** (14x20 mm) PACKAGE OUTLINE -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL :			
APPROVE		DOC. NO.	530-ASS-P004
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	Q128 - 1
		DATE	Apr. 1 1998
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